CLAIMS

What is claimed is:

1. A method comprising:

a) receiving a stream of bits in a first integrated circuit (IC) device, the stream represents a sequence of symbols transmitted by a second IC device over a serial point to point link that couples the first and second devices, wherein each of the symbols is M >1 bits long;

b) comparing a first M-bit section of the stream to a non-data symbol;

c) comparing a second M-bit section of the stream to the non-data symbol, the second section being offset by one bit in the stream relative to the first section;

d) if there is a match between the second section and the non-data symbol, then asserting a flag indicating symbol alignment and treating, in the first device, each of a plurality of consecutive, non-overlapping M-bit sections that immediately follow the second section to be a separate symbol; and

e) determining whether or not the plurality of M-bit sections that follow the second section are a predefined training sequence that has an instance of the non-data symbol, and if not then deasserting the flag to indicate no symbol alignment and if yes then sustaining the flag.

2. The method of claim 1 wherein the non-data symbol is designed to be unlikely to match any group of M consecutive bits in the stream unless the second device had knowledge that it was transmitting the non-data symbol.

3. The method of claim 1 wherein the non-data symbol is a PCI Express COM.

4. The method of claim 1 further comprising, after d):

comparing a group of symbols, received in the first device following the first section, to a group of training symbols, and if there is a mismatch between those two groups then deasserting the flag.

5. An integrated circuit (IC) device comprising:

an analog front end (AFE) to transmit and receive streams of information that represent sequences of M-bit symbols, the AFE being part of a serial point to point link between the IC device and another IC device; and

alignment logic that includes a) a section formation circuit to receive a stream of information from the AFE that was transmitted by said another IC device, the section formation circuit having M storage banks to capture a plurality of M-bit sections of the stream, respectively, each of the plurality of M-bit sections being offset by one bit in the stream relative to its adjacent section, b) a comparator circuit having an input coupled to the M storage banks, the comparator part to compare each of the captured plurality of M-bit sections to a stored non-data symbol value and in response provide M bank hit signals, c) a priority encoder circuit having an input coupled to receive the M bank hit signals, d) a multiplexer circuit having an input coupled to the M storage banks and a control input coupled to an output of the encoder circuit.

6. The integrated circuit of claim 5 wherein the alignment logic further comprises control logic coupled to the output of the comparator circuit to assert a lock signal in response to any of the M bank hit signals being asserted, the lock signal when asserted enables the multiplexer to select M-bit sections from one of the M storage banks indicated by the output of the encoder circuit.

7. The integrated circuit of claim 6 further comprising:

a link training state machine (LTSM) having an input coupled to an output of the multiplexer, the LTSM to begin checking the output of the multiplexer circuit for a predefined training sequence of symbols in response to the lock signal being asserted, and if the predefined training sequence is not detected within a predefined number of clock cycles following assertion of the lock signal, then signaling the control logic to deassert the lock signal.

8. The integrated circuit of claim 5 wherein the analog front end (AFE) is to receive streams of information, which represent sequences of M-bit symbols, in accordance with a receive clock, and the alignment logic is clocked by the receive clock.

9. The integrated circuit of claim 5 wherein the non-data symbol value is the value given to the COMma symbol under PCI Express.

10. A system comprising:

a processor;

a main memory; and

an integrated circuit (IC) device which is communicatively coupled to the processor and the main memory and provides the processor with I/O access, the IC device having link interface circuitry that supports a serial, point to point link, the circuitry having

an analog front end (AFE) to transmit and receive streams of information that represent sequences of M-bit symbols between the root complex and another device, where M is a positive integer greater than one, and

alignment logic that includes a) a section formation circuit to receive a stream of information from the AFE that was transmitted by said another device, the section formation circuit having M storage banks to capture a plurality of M-bit sections of the stream, respectively, each of the plurality of M-bit sections being offset by one bit in the stream relative to an adjacent section, b) a comparator circuit having an input coupled to the M storage banks, the comparator part to compare each of the captured plurality of M-bit sections to a stored non-data symbol value and in response provide M bank hit signals at its output, and c) a multiplexer circuit having an input coupled to the M storage banks and a control input coupled to the output of the comparator circuit.

11. The system of claim 10 wherein the alignment logic further comprises control logic coupled to the output of the comparator part to assert a lock signal in response to any of the M bank hit signals being asserted, the lock signal when asserted enables the multiplexer to select M-bit sections from one of the M storage banks.

12. The system of claim 10 further comprising:

a link training state machine (LTSM) having an input coupled to an output of the multiplexer, the LTSM to begin checking the output of the multiplexer for a training sequence of symbols in response to the lock signal

being asserted, and if the training sequence is not detected within a predefined number of clock cycles following assertion of the lock signal, then signaling the control logic to deassert the lock signal.

13. The system of claim 10 wherein the analog front end (AFE) is to receive streams of information, which represent sequences of M-bit symbols, in accordance with a receive clock, and the alignment logic is clocked by the receive clock.

14. The system of claim 10 further comprising a graphics element, and wherein the IC device is a graphics and memory controller hub (GMCH) that communicatively couples the processor to the main memory and the graphics element.

15. The system of claim 13 wherein the receive clock is derived by the AFE from a transmit clock that is embedded in a transmission by said another device.

16. The system of claim 10 wherein the IC device is an I/O controller hub (ICH) that communicatively couples the processor to peripheral devices.